APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/634,597	08/04/2003	Uri Cummings	FULCP009	6534

22434	7590	04/04/2006

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EXAMINER
TRAN, KHANH C

ART UNIT	PAPER NUMBER
2611	

DATE MAILED: 04/04/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)
Office Action Summary	10/634,597	CUMMINGS ET AL.
	Examiner	Art Unit	
	Khanh Tran	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>23 January 2006</u>.

2a)☒ This action is **FINAL**.   2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) <u>1-37</u> is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) <u>1,11-13,15,18,19,24 and 31-37</u> is/are rejected.

7)☒ Claim(s) <u>2-10,14,16,17,20-23 and 25-30</u> is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on <u>08/04/2003</u> is/are: a)☒ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☐ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
    Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____.

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____.

DETAILED ACTION

1. The Amendment filed on 01/23/2006 has been entered. Claims 1-37 are

pending in this Office action.

Response to Arguments

2. Applicant's arguments filed on 01/23/2006 have been fully considered but they

are not persuasive. See the explanation in claim 1 rejection.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set
> forth in section 102 of this title, if the differences between the subject matter sought to be patented and
> the prior art are such that the subject matter as a whole would have been obvious at the time the
> invention was made to a person having ordinary skill in the art to which said subject matter pertains.
> Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 11-13, 15 and 18 are rejected under 35 U.S.C. 103(a) as being

unpatentable over Benayoun et al. U.S. Patent Application Publication No. US

2002/0021694 A1.

Regarding claim 1, Benayoun et al. U.S. Patent Application Publication No. US

2002/0021694 A1 has become U.S. Patent 7,006,498 B2 and is referred to thereto in

the claim rejection below.

In response to Applicants' arguments that Benayoun et al. does not teach an integrated circuit, which includes various claimed elements as recited in claim 1.

The Examiner responds that Applicants' arguments are not persuasive. Benayoun et al. invention is directed to the transmission of data between local area networks (LANs) coupled by a *hub that further includes multiple LAN adapters* coupled to the LANs. Benayoun et al. further teaches an asynchronous transfer mode (ATM) crossbar switch coupling all LAN adapters; see paragraph [0007].

Figure 1 illustrates block diagram of an exemplary data transmission system including four local area networks (LANs) coupled by **a hub 15**. In paragraph [0015], a hub 15 includes *an asynchronous transfer mode (ATM) crossbar switch 18 and multiple LAN adapters 20, 22, 24 and 26*. The hub 15 corresponds to the claimed integrated circuit.

The LAN adapters 20, 22, 24 and 26, as recited above, correspond to a plurality of synchronous modules.

Benayoun et al. does not expressly teach a plurality of clock converters as set forth in the application claim.

However, referring to figure 4, see also paragraph [0008], Benayoun et al. teaches the requesting LAN adapter coupled to the LAN to transmit LAN data frame includes a *serial communication controller (SCC) 68* that further includes a means for converting the LAN data frame into serial data implemented as concatenated slots of the ATM cell size in the high-level data link control (HDLC) format before transmitting the serial data to the ATM crossbar switch. Because the serial communication controller

(SCC) 64 converts the LAN data frame into serial data implemented as concatenated

slots of the ATM cell size in the high-level data link control (HDLC) format before

transmitting the serial data to the ATM crossbar switch, one of ordinary skill in the would

have recognized the interchangeability of the serial communication controllers (SCC) 64

taught in Benayoun et al. invention for the clock domain converters specified in the

claim.

On pages 10-11 of Applicants' Remarks, Applicants' arguments that Benayoun et

al. ATM crossbar switch does not employ an asynchronous handshake protocol.

The Examiner responds that Applicants' arguments are not persuasive. In

paragraph [0016] and [0017], Benayoun et al. teaches a crossbar switch 18 operating in

asynchronous transfer mode (ATM) that includes a data switch module 30, a scheduler

32, multiple LAN adapter connectors 34 and 36 coupling multiple LANs to ATM crossbar

switch 18, scheduler 32 and to LAN adapter connectors 34 and 36. As recited above,

the serial communication controller (SCC) 64 converts the LAN data frame into serial

data implemented as concatenated slots of the ATM cell size in the high-level data link

control (HDLC) format before transmitting the serial data to the ATM crossbar switch or

vice versa [Emphasis Added]. As discussed above, the serial communication controllers

(SCC) 64 performs the function of the claimed clock converter. In light of the foregoing

teachings, *the serial communication controller (SCC) 64 converts the LAN data frame*

into serial data implemented as concatenated slots of the ATM cell size by transmission

of data according to an asynchronous handshake protocol as claimed in the application

claim.

In paragraph [0018], scheduler 32 also includes an algorithm unit 46, which determines the best data connection to establish each time a request is issued by a requesting LAN. Such a determination is based on the selection of the request amongst all requests received from the requesting LAN adapters that meets some predetermined criteria such as a priority order. As recited above, the crossbar switch 17 operates in asynchronous transfer mode, corresponding to the claimed asynchronous domain.

Benayoun et al. does not teach the ATM crossbar switch 18 implementing a first-in-first-out (FIFO) channel between any two of the clock domain converters.

As recited above, scheduler 32 also includes an algorithm unit 46, which determines the best data connection to establish each time a request is issued by a requesting LAN based on the selection of the request amongst all requests received from the requesting LAN adapters that meets some predetermined criteria such as a priority order or any other criteria defined by the user. Because Benayoun et al. teaches scheduler 32 determines the best data connection to establish each time a request being issued by a requesting LAN based on the selection of the request amongst all requests received from the requesting LAN adapters or any other criteria defined by the user, it would have been obvious for one of ordinary skill in the art at the time of the invention Benayoun et al. scheduler 32 could be modified to implement the ATM crossbar switch 18 such that scheduler 32 implements a first-in-first-out (FIFO) channel as claimed in the application claim.

Regarding claim 11, as recited in claim 1, In paragraph [0018], scheduler 32 also includes an algorithm unit 46, which determines the best data connection to establish each time a request is issued by a requesting LAN. Such a determination is based on the selection of the request amongst all requests received from the requesting LAN adapters that meets some predetermined criteria such as a priority order.

Regarding claim 12, in paragraph [0016], an ATM crossbar switch 18 that includes a clock generator 38 for supplying the clock and the synchronization to data switch module 30, scheduler 32. In view of that, the ATM crossbar switch 18 operates on one timing assumption.

Regarding claim 13, the clock generator 38 generates clock pulses; therefore, the timing assumption is based on pulse timing assumption.

Regarding claim 15, because crossbar switch 18 operates in asynchronous transfer mode, the asynchronous handshake protocol is delay-insensitive.

Regarding claim 18, as recited in claim 1, scheduler 32 also includes an algorithm unit 46, which determines the best data connection to establish each time a request is issued by a requesting LAN. Such a determination is based on the selection of the request amongst all requests received from the requesting LAN adapters that

meets some predetermined criteria such as a priority order. Hence, the requests include

requests to the same destination.

4. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over

Benayoun et al. U.S. Patent Application Publication No. US 2002/0021694 A1 as

applied to claim 18 and further in view of admitted prior art in the original disclosure.

Regarding claim 19, Benayoun et al. teaches a scheduler 32 for determining the

best data connection to establish each time a request is issued by a requesting LAN. In

view of that, the scheduler 32 corresponds to the claimed arbitration circuitry. Benayoun

et al., however, does not teach scheduler 32 comprising at least one Seitz arbiter.

Admitted prior art in the original disclosure discloses implementations of Seitz arbiter

and QFR circuits in C. L. Seitz, System Timing, chapter 7, pp. 218-262, Reading,

Mass., Addison-Wesley, 1980, and F. U. Rosemberger, C. E. Molnar, T. J. Chaney, and

T. P. Fang, Q-modules: Internally clocked delay-insensitive modules, IEEE Trans.,

Computers, vol. 37, no.9, pp. 1005-1018, September 1988, respectively; see column

54, line 23 via column 55, line 5, of the original disclosure. Because of known potential

benefits of Seitz arbiter, one of ordinary skill in the art would have been motivated to

implement Seitz arbiter, as taught by admitted prior art, into crossbar switch as taught

by Benayoun et al.. Furthermore, implementation of new intended use (e.g. Seitz

arbiter) for an old product does not make a claim to that old product patentable. In re

Schreiber, 44 USPQ2d (Fed. Cir. 1997).

5. Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over
Benayoun et al. U.S. Patent Application Publication No. US 2002/0021694 A1 as
applied to claim 1 above, and further in view of Chou et al. U.S. Patent 6,763,418.

Regarding claim 24, Benayoun et al. does not teach a build-in-self-test (BIST)
module as set forth in the claim. Chou et al. discloses in figures 2A and 2B a data path
20 includes crossbar 22 to which eight communication ports 24 are coupled. Figure 2A
shows an arbiter 36. In addition of eight communication ports 24, a management port 26
and a functional BIST port 28 are also coupled to crossbar 22; see figure 2B. Benayoun
et al. and Chou et al. teachings are in the same field of endeavor. Chou et al. invention
differs from Benayoun et al. invention in that Chou et al. teachings include a functional
BIST port. In light of Chou et al. teachings, it would have been obvious for one of
ordinary skill in the art at the time the invention was made that Wicki et al. crossbar
switch can be modified to include a BIST as taught by Chou et al.. Motivation is that the
BIST can be used for testing data transmission between the interfaces through crossbar
switch.

6. Claim 31 is rejected under 35 U.S.C. 103(a) as being unpatentable over
Benayoun et al. U.S. Patent Application Publication No. US 2002/0021694 A1 as
applied to claim 1 above, and further in view of Barber et al. U.S. Patent 4,849,751.

Regarding claim 31, Benayoun et al. does not teach the crossbar switch is
implemented on a CMOS integrated circuit as set forth in the application claim. Barber
et al., nevertheless, teaches a CMOS integrated circuit digital crossbar switching

arrangement shown in figure 5 of another US Patent. CMOS technology is mature and

well known in the art. Because of the potential known benefits of CMOS technology,

one of ordinary skill in the art at the time the invention was made would have been

motivated to implement Benayoun et al. ATM crossbar switch including crossbar unit on

a CMOS integrated circuit as taught in Barber et al. invention.

7. Claims 32-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Benayoun et al. U.S. Patent Application Publication No. US 2002/0021694 A1 as

applied to claim 1 above, and further in view of Butts et al. U.S. Patent 6,002,861.

Regarding claim 32, Benayoun et al. does not teach a computer-readable

medium having data structures stored representative of the computer-bus switch

architecture. However, as well known in the art of digital logic network design, one

performs simulation of functional circuit design before actually building the digital logic

network permanently. Butts et al. discusses such simulation in another US patent,

wherein a method is disclosed for performing simulation of functional circuit design

using a hardware and software emulation system. As disclosed in the abstract, Butts et

al. teachings utilize a plurality of electronically reconfigurable gate array logic chips

interconnected via a reconfigurable interconnect, which comprises a partial crossbar.

The reconfigurable interconnect permits the digital network realized on the

interconnected chips to be changed at will. Since Butts et al. teachings are in the same

field of endeavor, and utilizes same components (e.g. logic chips, reconfigurable

crossbar, ...) to simulate a digital network in the design, one of ordinary skill in the art

would have been motivated to implement computer instructions stored a computer readable medium as data structures to simulate Benayoun et al. teachings, as part of the preliminary design before actual implementation.

Regarding claim 33, said claim is rejected on the same ground as for claim 32 because the claimed simulatable representation is discussed in claim 32.

Regarding claim 34, figure 43 in Butts et al. invention illustrates a block diagram of a Realizer design conversion system including netlists for logic chips. The Realizer design conversion system is part of hardware and software emulation system taught in Butts et al. invention.

Regarding claim 35, as recited in claim 32, Butts et al. discloses a method for performing simulation of a digital logic network as part of design using a hardware and software emulation system. In view of that, one of ordinary skill in the art would have recognized that the data structures as part of the hardware and software emulation system can be implemented to include code description representative of Benayoun et al. teachings.

Regarding claim 36, using analogous argument as for claim 35, the code description would correspond to a hardware description language as part of the hardware and software emulation system.

Regarding claim 37, as discussed in claim 32, since Butts et al. teachings utilize a plurality of electronically reconfigurable gate array logic chips interconnected via a reconfigurable crossbar, corresponding to the claimed set of semiconductor processing masks, it would have been obvious for one of ordinary skill in the art that the logic chips and reconfigurable crossbar as taught by Butts et al. can be implemented to represent at least a portion of Benayoun et al. teachings.

Allowable Subject Matter

8. Claims 2-10, 14, 16-17, 20-23, 25-30 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

9.**THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khanh Tran whose telephone number is 571-272-3007. The examiner can normally be reached on Monday - Friday from 08:00 AM - 05:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay Patel can be reached on 571-272-2988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KCT   *Khanh cong Tran*   04/02/2006

Primary Examiner   KHANH TRAN